

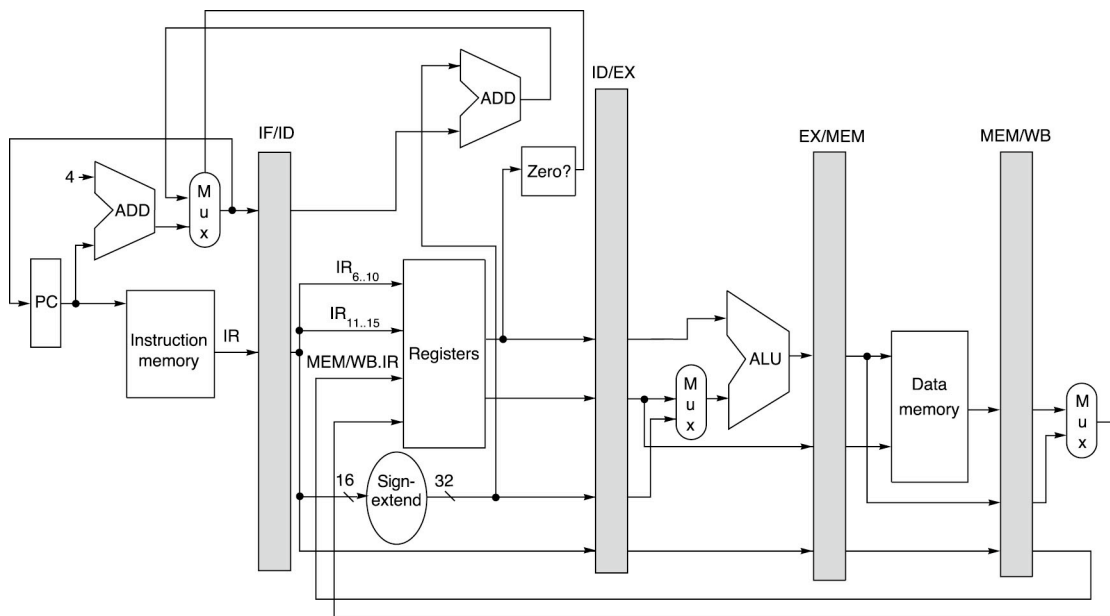
Assignment #2 – Static Pipeline

You have 1 week to complete the assignment, the due date being June 10th, in class.

Question

For the following questions assume the classic 5-stage pipeline architecture of figure 1.

All memory accesses take 1 clock cycle and half cycle clocking is available for WB – ID General Purpose Register references.



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Figure 1 – Classic 5-stage pipeline.

All questions refer to the following code in which the initial value for register R4 is 231 – R8.

```
Loop:      R2 ← Mem[ 0 + R8 ]
           R2 ← R2 + 1
           Mem[ 0 + R8 ] ← R2
           R8 ← R8 - 3
           R1 ← R4 + R8
           IF (R1 != 0) THEN goto 'Loop'
```

1. Compose a pipeline-timing diagram for the case of a pipeline without forwarding (blank timing diagrams attached). The hardware assumes (predicts) that the branch will not be taken. How many cycles are necessary to complete the loop?
2. Now provide a pipeline-timing diagram for the case of forwarding and branch delay slot enabled. Moreover, you are also permitted to reorder instructions / modify operands for the purpose of utilizing the branch delay slot. You may reorder instructions and modify individual instruction operands. How many cycles are necessary to complete your optimized code?