

Example – ISA

Question #1

Consider the cost of adding a register-memory addressing mode to a load-store machine. Thus, the load-store sequence,

LOAD	R1, 0(Rb)	$R1 \leftarrow M[0, Rb]$
ADD	R2, R2, R1	$R2 \leftarrow R2 + R1$

Might be replaced with,

ADD	R2, 0(Rb)	$R2 \leftarrow R2 + M[0 + Rb]$
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Assume that the new instruction causes an increase of 10% in the clock period.

Instruction frequencies (i.e. %) under the target application are defined as per the following table.

Load	Store	Add	Sub	Mul	Comp	Load imm	Branch	Jmp	Call	Rtn	Shift	And	Or	Other
22.8	14.3	14.6	0.5	0.1	12.4	6.8	11.5	1.3	1.1	1.5	6.2	1.6	4.2	0.5

Assuming that the new instruction has no effect on CPI, what percentage of load instructions (under the old architecture) must be replaced with the new load-execute instruction for performance of the old and new configuration to remain unchanged?

Question #2

After studying traces from your favoured benchmark applications, procedure calls are identified as one of the most expensive operations.

A scheme is devised for reducing the load-store operation normally associated with procedure calls and returns.

- Clock frequency of the unoptimized version is 5% higher;
- 30% of instructions in the unoptimized version are load-stores;
- The optimized version uses 2/3 the load stores as in the unoptimized. In all other instructions the execution counts are unchanged;
- All instructions take one clock cycle.

Which machine is the faster and by how much?