

Appendix – Timing diagrams

Pipeline Timing Diagram – Example #1

Speculative execution, NO superscalar, BNE still resolved in integer ALU, BTB and predict taken

Instruction	Clock Cycle																							
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
Load	F	D	I	EX	EM	W	C																	
Add		F	D	I	-	-	EF	EF	EF	W	C													
Store			F	D	I	EX	-	-	-	-	WS	C												
Sub				F	D	I	EX	W	-	-	-	-	C											
BNE					F	D	I	-	R	-	-	-	-	C										
Load						F	D	I	EX	EM	W	-	-	-	C									
Add							F	D	I	-	-	EF	EF	EF	W	C								
Store								F	D	I	EX	-	-	-	-	WS	C							
Sub									F	D	I	EX	W	-	-	-	-	C						
BNE										F	D	I	-	R	-	-	-	-	C					
Load											F	D	I	EX	EM	W	-	-	-	C				
Add												F	D	I	-	-	EF	EF	EF	W	C			
Store													F	D	I	EX	-	-	-	-	WS	C		
Sub														F	D	I	EX	W	-	-	-	-	C	
BNE															F	D	I	-	R	-	-	-	-	C

Pipeline Timing Diagram – Example #1

Speculative execution, Superscalar (dual), BNE still resolved in integer ALU, BTB and predict taken

Instruction	Clock Cycle																							
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
Load	F	D	I	EX	EM	W	C																	
Add	F	D	I	-	-	-	EF	EF	EF	W	C													
Store		F	D	I	EX	-	-	-	-	-	WS	C												
Sub		F	D	I	-	EX	W	-	-	-	-	-	C											
BNE			F	D	I	-	R	-	-	-	-	-	-	C										
Load				F	D	I	EX	EM	W	-	-	-	-	-	C									
Add				F	D	I	-	-	-	EF	EF	EF	W	-	-	C								
Store					F	D	I	EX	-	-	-	-	-	WS	-	-	C							
Sub					F	D	I	-	EX	W	-	-	-	-	-	-	-	C						
BNE						F	D	I	-	R	-	-	-	-	-	-	-	-	C					
Load							F	D	I	EX	EM	W	-	-	-	-	-	-	-	C				
Add							F	D	I	-	-	-	EF	EF	EF	W	-	-	-	-	C			
Store								F	D	I	EX	-	-	-	-	-	WS	-	-	-	-	-	C	
Sub								F	D	I	-	EX	W	-	-	-	-	-	-	-	-	-	-	C
BNE									F	D	I	-	R	-	-	-	-	-	-	-	-	-	-	C

Pipeline Timing Diagram – Example #2

Superscalar (dual), Independent ALU for Integer, Address and Branch resolution. Up to two write-backs per clock cycle, BTB and predict taken.

Instruction	Clock Cycle																								
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
Load	F	D	I	E1	EM	W																			
Add	F	D	I	-	-	-	EX	W																	
Store		F	D	I	E1	-	-	-	EM																
Add		F	D	I	EX	W																			
BNE			F	D	I	-	-	-	R																
Load				F	D	I	-	-	-	E1	EM	W													
Add				F	D	I	-	-	-	-	-	-	EX	W											
Store					F	D	I	-	-	-	E1	-	-	-	EM										
Add					F	D	I	-	-	EX	W														
BNE						F	D	I	-	-	-	-	-	-	R										
Load							F	D	I	-	-	-	-	-	-	E1	EM	W							
Add							F	D	I	-	-	-	-	-	-	-	-	-	EX	W					
Store								F	D	I	-	-	-	-	-	-	E1	-	-	-	EM				
Sub								F	D	I	-	-	-	-	-	EX	W								
BNE									F	D	I	-	-	-	-	-	-	-	-	-	R				

Address, Integer and Branch ALUs are independent. Also assume that write back of up to two instructions also supported between different functional units (implies a write buffer to cache is available).

Pipeline Timing Diagram – Example #2

Superscalar (dual), Speculative, Independent ALU for Integer, Address and Branch resolution. Up to two write-backs per clock cycle, BTB and predict taken.

Instruction	Clock Cycle																							
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
Load	F	D	I	E1	EM	W	C																	
Add	F	D	I	-	-	-	EX	W	C															
Store		F	D	I	E1	-	-		C															
Add		F	D	I	EX	W			C															
BNE			F	D	I	-	-	-	R	C														
Load				F	D	I	E1	EM	W		C													
Add				F	D	I				EX	W	C												
Store					F	D	I	E1				C												
Add					F	D	I	EX	W			C												
BNE						F	D	I	-	-		R	C											
Load							F	D	I	E1	EM	W		C										
Add							F	D	I				EX	W	C									
Store								F	D	I	-				C									
Sub								F	D	I	-	W				C								
BNE									F	D	I	-	-		R	C								

Store memory accesses is buffered, thus as soon as write for the corresponding ‘Add’ instruction has completed we forward the corresponding value to the cache write buffer as part of commit.